Amendments to the Claims:

The following listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) A sampling clock generation circuit that generates a sampling clock used for sampling data, the sampling clock generation circuit comprising:

an edge detection circuit detecting between which two clock edges a data edge is located, the two edges being among edges of first to N-th clocks having the same frequency but mutually different phases, the edge detection circuit comprising:

a first holding circuit that holds data by using the first clock, a J-th holding circuit that holds data by using a J-th clock (where: $1 < J < N$), and an N-th holding circuit that holds data by using the N-th clock;

a first detection circuit that detects whether or not there is a data edge between the edges of the first clock and a second clock, based on data held in the first holding circuit and a second holding circuit, a J-th detection circuit that detects whether or not there is a data edge between the edges of the J-th clock and a $(J + 1)$-th clock, based on data held in the J-th holding circuit and a $(J + 1)$-th holding circuit, and an N-th detection circuit that detects whether or not there is a data edge between the edges of the N-th clock and the first clock, based on data held in the N-th and first holding circuits; and

a clock selection circuit that selects one clock from among the first to N-th clocks, based on detection information from the edge detection circuit from the first to N-th detection circuits, and outputs the selected clock as the sampling clock,

when a set-up time of the first to N-th holding circuits is TS, a hold time of the first to N-th holding circuits is TH, and a period of each of the first to N-th clocks is T, number of clocks N of the first to N-th clocks being such that: $N \leq [T/(TS + TH)]$ (where $[T/(TS + TH)]$ is a maximum integer that does not exceed $T/(TS+TH)$);

a clock generation circuit that includes an oscillation circuit and generates the first to N-th clocks,

the oscillation circuit comprising:

inversion circuits that are connected serially; and

buffer circuits,

an output of each of the inversion circuits being connected to an input of a corresponding buffer circuit among the buffer circuits,

an output of a final-stage inversion circuit among the inversion circuits being connected to an input of an initial-stage inversion circuit among the inversion circuits via a feedback line,

the inversion circuits being disposed along a first line that is parallel to the feedback line,

the buffer circuits being disposed along a second line that is ~~parallels~~ parallel to the feedback line but differs from the first ~~line.~~ line, and

the feedback line being disposed in a region between the inversion circuits and the buffer circuits.

2-3. (Canceled)

4. (Previously Presented) The sampling clock generation circuit as defined by claim 1,

number of clocks N being such that N = [T/(TS + TH)] (where [T/(TS + TH)] is a maximum integer that does not exceed T/(TS+TH)).

5. (Previously Presented) The sampling clock generation circuit as defined by claim 1,

the number of clocks N of the first to N-th clocks being such that N = 5.

6-7. (Canceled)

8. (Previously Presented) The sampling clock generation circuit as defined by claim 1,

the clock selection circuit selecting from the first to N-th clocks a clock having an edge that is shifted by a given set number M of edges from a data edge, and outputting the selected clock as the sampling clock.

9. (Previously Presented) The sampling clock generation circuit as defined by claim 8,

the number M being set to a number that ensures a set-up time and a hold time of a circuit that holds data based on the generated sampling clock.

10. (Currently Amended) A sampling clock generation circuit that generates a sampling clock used for sampling data, the sampling clock generation circuit comprising:

an edge detection circuit that detects a data edge; and

a clock selection circuit that selects a clock from among first to N-th clocks having the same frequency but mutually different phases, based on detection information from the edge detection circuit, and outputs the selected clock as the sampling clock,

the edge detection circuit comprising at least one holding circuit that holds data at any clock from among the first to N-th clocks, and

when a set-up time of the holding circuit comprised by the edge detection circuit is TS, a hold time of the holding circuit comprised by the edge detection circuit is TH, and a period of each of the first to N-th clocks is T, number of clocks N of the first to N-th clocks being such that: $N \leq [T/(TS + TH)]$ (where $[T/(TS + TH)]$ is a maximum integer that does not exceed $T/(TS+TH)$);

a clock generation circuit that includes an oscillation circuit and generates the first to N-th clocks,

the oscillation circuit comprising:

inversion circuits that are connected serially; and

buffer circuits,

an output of each of the inversion circuits being connected to an input of a corresponding buffer circuit among the buffer circuits,

an output of a final-stage inversion circuit among the inversion circuits being connected to an input of an initial stage inversion circuit among the inversion circuits via a feedback line,

the inversion circuits being disposed along a first line that is parallel to the feedback line,

the buffer circuits being disposed along a second line that is parallel to the feedback line but differs from the first ~~line.~~ line, and

the feedback line being disposed in a region between the inversion circuits and the buffer circuits.

11. (Previously Presented) The sampling clock generation circuit as defined by claim 10,

number of clocks N being such that N = [T/(TS + TH)] (where [T/(TS + TH)] is a maximum integer that does not exceed T/(TS+TH)).

12. (Previously Presented) The sampling clock generation circuit as defined by claim 10,

the number of clocks N of the first to N-th clocks being such that N = 5.

13. (Previously Presented) The sampling clock generation circuit as defined by claim 11,

the number of clocks N of the first to N-th clocks being such that N = 5.

14. (Previously Presented) A sampling clock generation circuit as defined by claim 10,

the clock selection circuit selecting from the first to N-th clocks a clock having an edge that is shifted by a given set number M of edges from the data edge, and outputting the selected clock as the sampling clock.

15. (Previously Presented) The sampling clock generation circuit as defined by claim 14,

the number M being set to a number that ensures a set-up time and a hold time of a circuit that holds data based on the generated sampling clock.

16. (Previously Presented) The sampling clock generation circuit as defined by claim 1, further comprising:

a PLL circuit having an oscillation circuit with a variably-controlled oscillation frequency, and phase-synchronizing a clock generated by the oscillation circuit with a base clock,

the first to N-th clocks being generated based on outputs of first to N-th inversion circuits of an odd number of stages included in the oscillation circuit.

17. (Previously Presented) The sampling clock generation circuit as defined by claim 10, further comprising:

a PLL circuit having an oscillation circuit with a variably-controlled oscillation frequency, and phase-synchronizing a clock generated by the oscillation circuit with a base clock,

the first to N-th clocks being generated based on outputs of first to N-th inversion circuits of an odd number of stages included in the oscillation circuit.

18. (Canceled)

19. (Previously Presented) The sampling clock generation circuit as defined by claim 16,

at least one of a disposition of the first to N-th inversion circuits and interconnection of output lines of the first to N-th inversion circuits being performed in such a manner that phase differences between the first to N-th clocks are equal.

20. (Previously Presented) The sampling clock generation circuit as defined by claim 17,

at least one of a disposition of the first to N-th inversion circuits and interconnection of output lines of the first to N-th inversion circuits being performed in such a manner that phase differences between the first to N-th clocks are equal.

21. (Canceled)

22. (Previously Presented) The sampling clock generation circuit as defined by claim 16,

lines for the first to N-th clocks being interconnected in such a manner that the parasitic capacitances of lines of the first to N-th clocks are equal.

23. (Previously Presented) The sampling clock generation circuit as defined by claim 17,

lines for the first to N-th clocks being interconnected in such a manner that the parasitic capacitances of lines of the first to N-th clocks are equal.

24. (Canceled)

25. (Previously Presented) A data transfer control device for providing data transfer over a bus, the data transfer control device comprising:

the sampling clock generation circuit as defined by claim 1; and

a circuit that holds data, based on the sampling clock generated by the sampling clock generation circuit, and performs given processing for data transfer, based on the held data.

26. (Previously Presented) A data transfer control device for providing data transfer over a bus, the data transfer control device comprising:

the sampling clock generation circuit as defined by claim 10; and

a circuit that holds data, based on the sampling clock generated by the sampling clock generation circuit, and performs given processing for data transfer, based on the held data.

27. (Canceled)

28. (Previously Presented) The data transfer control device as defined by claim 25,

data transfer being in accordance with the Universal Serial Bus (USB) standard.

29. (Previously Presented) The data transfer control device as defined by claim 26,

data transfer being in accordance with the Universal Serial Bus (USB) standard.

30. (Canceled)

31. (Previously Presented) Electronic equipment comprising:

the data transfer control device as defined by claim 25; and

a device that performs output processing, fetch processing or storage processing on data transferred through the data transfer control device and the bus.

32. (Previously Presented) Electronic equipment comprising:

the data transfer control device as defined by claim 26; and

a device that performs output processing, fetch processing or storage processing on data transferred through the data transfer control device and the bus.

33. (Canceled)

34. (Previously Presented) Electronic equipment comprising:

the data transfer control device as defined by claim 28; and

a device that performs output processing, fetch processing or storage processing on data transferred through the data transfer control device and the bus.

35. (Previously Presented) Electronic equipment comprising:

the data transfer control device as defined by claim 29; and

a device that performs output processing, fetch processing or storage processing on data transferred through the data transfer control device and the bus.

36-40. (Canceled)

41. (New) A sampling clock generation circuit that generates a sampling clock used for sampling data, the sampling clock generation circuit comprising:

an edge detection circuit detecting between which two clock edges a data edge is located, the two edges being among edges of first to N-th clocks having the same frequency but mutually different phases, the edge detection circuit comprising:

a first holding circuit that holds data by using the first clock, a J-th holding circuit that holds data by using a J-th clock (where: $1 < J < N$), and an N-th holding circuit that holds data by using the N-th clock;

a first detection circuit that detects whether or not there is a data edge between the edges of the first clock and a second clock, based on data held in the first holding circuit and a second holding circuit, a J-th detection circuit that detects whether or not there is a data edge between the edges of the J-th clock and a (J + 1)-th clock, based on data held in the J-th holding circuit and a (J + 1)-th holding circuit, and an N-th detection circuit that detects whether or not there is a data edge between the edges of the N-th clock and the first clock, based on data held in the N-th and first holding circuits; and

a clock selection circuit that selects one clock from among the first to N-th clocks, based on detection information from the edge detection circuit from the first to N-th detection circuits, and outputs the selected clock as the sampling clock,

when a set-up time of the first to N-th holding circuits is TS, a hold time of the first to N-th holding circuits is TH, and a period of each of the first to N-th clocks is T, number of clocks N of the first to N-th clocks being such that: $N \leq [T/(TS + TH)]$ (where $[T/(TS + TH)]$ is a maximum integer that does not exceed $T/(TS+TH)$);

a clock generation circuit that includes an oscillation circuit and generates the first to N-th clocks,

the oscillation circuit comprising:

inversion circuits that are connected serially; and

buffer circuits,

an output of each of the inversion circuits being connected to an input of a corresponding buffer circuit among the buffer circuits,

an output of a final-stage inversion circuit among the inversion circuits being connected to an input of an initial-stage inversion circuit among the inversion circuits via a feedback line,

the inversion circuits being disposed along a first line that is parallel to the feedback line,

the buffer circuits being disposed along a second line that is parallel to the feedback line but differs from the first line, and

the dummy lines and the feedback line being disposed in the region between the inversion circuits and the buffer circuits, each of the dummy lines being connected to the output of each of the inversion circuits.

42. (New) A sampling clock generation circuit that generates a sampling clock used for sampling data, the sampling clock generation circuit comprising:

an edge detection circuit that detects a data edge; and

a clock selection circuit that selects a clock from among first to N-th clocks having the same frequency but mutually different phases, based on detection information from the edge detection circuit, and outputs the selected clock as the sampling clock,

the edge detection circuit comprising at least one holding circuit that holds data at any clock from among the first to N-th clocks, and

when a set-up time of the holding circuit comprised by the edge detection circuit is TS, a hold time of the holding circuit comprised by the edge detection circuit is TH, and a period of each of the first to N-th clocks is T, number of clocks N of the first to N-th clocks being such that: $N \leq [T/(TS + TH)]$ (where $[T/(TS + TH)]$ is a maximum integer that does not exceed $T/(TS+TH)$);

a clock generation circuit that includes an oscillation circuit and generates the first to N-th clocks,

the oscillation circuit comprising:

inversion circuits that are connected serially; and

buffer circuits,

an output of each of the inversion circuits being connected to an input of a corresponding buffer circuit among the buffer circuits,

an output of a final-stage inversion circuit among the inversion circuits being connected to an input of an initial stage inversion circuit among the inversion circuits via a feedback line,

the inversion circuits being disposed along a first line that is parallel to the feedback line,

the buffer circuits being disposed along a second line that is parallel to the feedback line but differs from the first line, and

the dummy lines and the feedback line being disposed in the region between the inversion circuits and the buffer circuits, each of the dummy lines being connected to the output of each of the inversion circuits.